

**IN THE CLAIMS:**

1. (Previously Amended) A semiconductor device comprising:
  - a first interlayer insulating layer;
  - a plurality of wiring lines which are formed of Cu whose concentration is equal to or higher than  $10^{19}$  atoms/cm<sup>3</sup>, said plurality of wiring lines formed on said first interlayer insulating layer;
  - an insulating layer which has a property that Cu is unlikely to enter said insulating layer and which insulates between said plurality of wiring lines; and
  - a second interlayer insulating layer formed on said insulating layer having a property that Cu is unlikely to enter therein.
2. (Previously Amended) The semiconductor device according to claim 1, wherein said insulating layer comprises HSQ (Hydrogen Silsesquioxane).
3. (Previously Canceled)
4. (Previously Amended) A semiconductor device according to claim 1, further comprising:
  - at least one adhesion layer formed in an interface between said plurality of wiring lines and said insulating layer, said at least one adhesion layer allowing said plurality of wiring lines and said insulating layer to adhere to one another,
  - wherein each said at least one adhesion layer has a polishing rate which is essentially equivalent to a polishing rate of said plurality of wiring lines.

5. (Previously Amended) The semiconductor device according to claim 4, wherein at least one of said at least one adhesion layer comprises tungsten.

6-13. (Previously Canceled)

14. (Previously Added) A semiconductor device comprising:

a multi-layer insulating layer, comprising:

a middle layer comprised of PAE (Poly Arylene Ether);

an upper insulating layer and a lower insulating layer between which said middle layer is sandwiched, said upper and lower layers each comprised of HSQ (Hydrogen Silsesquioxane); and

an opening formed in a predetermined position in said PAE layer and said HSQ layers; and

a wiring line formed within said opening, said wiring line comprised of Cu having a concentration equal or higher than  $10^{19}$  atoms/cm<sup>3</sup>, said upper insulating layer and said lower insulating layer thereby forming an insulating layer which has a property that Cu is unlikely to enter said insulating layer.

15. (Previously Added) A semiconductor device comprising:

a first interlayer insulating layer;

a first layer of low permittivity material formed on said first interlayer insulating layer, said low permittivity material having a property that a migration of copper is limited in said material;

a first plurality of sections of copper being embedded in said first layer of low permittivity material;

a second interlayer insulating layer formed on said layer of low permittivity material, wherein said first interlayer insulating layer and said second interlayer insulating layer have a property in strength that offsets a property in strength of said first layer of low permittivity material.

16. (Previously Added) The semiconductor device of claim 15, wherein said first interlayer insulating layer and said second interlayer insulating layer each comprise SiN<sub>x</sub> and said first layer of low permittivity material comprises hydrogen silsesquixane (HSQ).

17. (Currently Added) The ~~semiconductive~~ semiconductor device of claim 16, further comprising:

a bottom layer formed below said first interlayer insulating layer, said bottom layer having at least one copper conductor line,

wherein said first interlayer insulating layer has a hole formed therein, said hole allowing at least one copper conductor line in said bottom layer to connect with one of said first plurality of sections of copper embedded in said first layer of low permittivity material.

18. (Previously Added) The semiconductor device of claim 17, further comprising:

a layer of adhesive material being formed at an interface between said first layer of low permittivity material and each of said first plurality of sections of copper being embedded therein.

19. (Previously Added) The semiconductor device of claim 18, wherein said adhesive material comprises tungsten (W).

20. (Previously Added) The semiconductor device of claim 15, further comprising:

a third interlayer insulating layer formed on said second interlayer insulating layer;

a second layer of low permittivity material formed on said third interlayer insulating layer, said low permittivity material having a property that a migration of copper is limited in said low permittivity material;

a second plurality of sections of copper being embedded in said second layer of low permittivity material; and

a fourth interlayer insulating layer formed on said second layer of low permittivity material.

21. (Previously Added) The semiconductor device of claim 20, wherein said first interlayer insulating layer, said second interlayer insulating layer, said third interlayer insulating layer, and said fourth interlayer insulating layer each comprising SiN, and

wherein said first layer of low permittivity material and said second layer of low permittivity material each comprises hydrogen silsesquixane (HSQ).

22. (Previously Added) The semiconductor device of claim 20, further comprising:

a layer of adhesive material formed at an interface between said second layer of low permittivity material and each of said second plurality of sections of copper being embedded therein.

23. (Previously Added) The semiconductor device of claim 22, wherein said adhesive material comprises tungsten (W).

24. (Previously Added) The semiconductive device of claim 20, said third interlayer insulating layer has a hole formed therein, said hole allowing a one of said first plurality of sections of copper to connect with one of said second plurality of sections of copper.

25. (New) A semiconductor device comprising:

a first interlayer insulating layer comprised of a first material;

a middle insulating layer on said first interlayer insulating layer, said middle insulating layer comprising an organic polymer;

at least one copper wiring section embedded in said middle insulating layer; and

a second interlayer insulating layer formed on said middle insulating layer, said second interlayer insulating layer comprised of said first material,

wherein said first interlayer insulating layer, said middle insulating layer, and said second interlayer insulating layer form a system that serves to confine a migration of copper ions from said at least one copper wiring section to be within said middle insulating layer.

26. (New) The device of claim 25, wherein said first material comprises SiN, and said middle insulating layer comprises hydrogen silsesquixane (HSQ), said HSQ having a property that a migration of copper ions is limited therein.

27. (New) The device of claim 25, wherein said first material comprises hydrogen silsesquixane (HSQ), and said middle insulating layer comprises Poly Arylene Ether (PAE), said HSQ having a property that a migration of copper ions is limited therein so that said first interlayer insulating layer thereby provides a lower layer to confine said migration of copper ions and said second interlayer insulating layer thereby provides an upper layer to confine said migration of copper ions.